UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,730	08/31/2001	Satoshi Itoi	PF-2861	8413

466 7590 08/23/2004

YOUNG & THOMPSON
745 SOUTH 23RD STREET 2ND FLOOR
ARLINGTON, VA 22202

EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/942,730	ITOI, SATOSHI
	Examiner	Art Unit
	Guy J. Lamarre, P.E.	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicants' IDS and priority paper of 01/2/2002 have been entered. The Examiner has considered the IDS.

1.1 Pursuant to 35 USC 131, **Claims 1-50** are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2.1 **Claims 1-50** are rejected under 35 U.S.C. 102(e) as being anticipated by **Yamawaki et al.** (US Patent No. 6,158,038; Sept. 15, 1997).

As per Claims 1-50, Yamawaki et al. discloses Reed-Solomon coding or ECC means with inner/outer coding means over Galois field means for data processing wherein length of data or codes are not restricted to a particular size and thus anticipates instant claims, and wherein preferred embodiments specify codes of interest along with particular coding structures, e.g., in Figs. 1, 3, 9-12 and 21 and related description, in conjunction with associated data buffering or table means. **Examiner** also notes that any number is a multiply of any other number even though a number is not necessary an integer multiply or integer multiple of another number.

As per Claim 1, in col. 2 line 40-42 et seq., e.g., Yamawaki et al. discloses method of implementing at least one of recording and transmitting digital data, under conditions that a total code length including data and error correcting codes corresponds to not less than 256 symbols, and each of said symbols comprises n-bits, where n is larger than 8.

As per Claim 2,in col. 2 line 40-42, Fig. 1, e.g.,. Yamawaki et al. discloses method as claimed in claim 1, further comprising the steps of: arraying said data and said error correcting codes in a matrix of plural rows and plural columns; calculating external code error correcting codes for all

column-directional alignments of data in a column direction, and further internal code error correcting codes for all row-directional alignments of data in a column direction or the external code error correcting codes; and recording the data and the calculated external and internal code error correcting codes.

As per Claim 3, in col. 5 lines 44, Yamawaki et al. discloses method as claimed in claim 1, wherein said error correcting codes are Reed-Solomon codes over GF (2.sup.n).

As per Claim 4, in col. 2 line 40-42, e.g., Yamawaki et al. discloses method as claimed in claim 1, wherein said data are arrayed in a matrix of plural rows and plural columns, and a total data length corresponds to a number of symbols, which is equal to or multiply of 2064.

As per Claim 5, in col. 2 line 40-42, e.g., Yamawaki et al. discloses method as claimed in claim 1, wherein said data are arrayed in a matrix of plural rows and plural columns, and a total data length corresponds to a number of symbols which is equal to or multiply of 33024.

As per Claim 6, in col. 2 line 40-42, e.g., Yamawaki et al. discloses method as claimed in claim 1, wherein said data are arrayed in a matrix of plural rows and plural columns, and a total data length of the rows corresponds to a number of symbols which is equal to or multiply of 192.

As per Claim 7, in col. 2 line 40-42, e.g., Yamawaki et al. discloses method as claimed in claim 1, wherein said data are arrayed in a matrix of plural rows and plural columns, and a total data length of the columns corresponds to a number of symbols which is equal to or multiply of 172.

As per Claim 8, in col. 2 line 40-42, e.g., Yamawaki et al. discloses method as claimed in claim 2, wherein external code error correcting codes are isolated into a first block comprising even number rows and a second block comprising odd number rows.

As per Claim 9. Yamawaki et al. discloses method as claimed in claim 8, wherein calculations of said external code error correcting codes are made with a row-directional increment of 2 or more integer in col. 2 line 40-42 et seq.

As per Claim 10. Yamawaki et al. discloses method as claimed in claim 1, wherein calculations of said error correcting codes are made with a second column-directional increment of 2 or more integer in col. 2 lines 40-42 et seq.

As per Claim 11. Yamawaki et al. discloses method as claimed in claim 1, further comprising the steps of: arraying said data and said error correcting codes in a matrix array of plural rows and plural columns; dividing said data and said error correcting codes into a plurality of sectors; and adding at least an additional information to each of said sectors to form each logic segment in col. 2 lines 40-42 et seq.

As per Claim 12. Yamawaki et al. discloses method as claimed in claim 11, wherein said each segment has a segment size of 2048 bytes in col. 2 line 40-42 et seq.

As per Claim 13. Yamawaki et al. discloses method as claimed in claim 11, wherein said each segment has a segment size of 2064 bytes, which comprises 2048 bytes for data and 16 bytes for segment header in col. 2 lines 40-42 et seq.

As per Claim 14. Yamawaki et al. discloses method as claimed in claim 11, wherein each external code error correcting code is placed following to an end of said each sector in col. 2 line 40-42 et seq.

As per Claim 15. Yamawaki et al. discloses method as claimed in claim 11, wherein each external code error correcting code is placed on a center region of said matrix array.

As per Claim 16. Yamawaki et al. discloses method as claimed in claim 15, wherein a length of said each symbol is equal to a bit length of coded data in col. 2 line 40-42 et seq.

As per Claim 17. Yamawaki et al. discloses method of preparing a table including at least data and error correcting codes, wherein a total code length including said data and said error correcting codes corresponds to not less than 256 symbols, and each of said symbols comprises n-bits, where n is larger than 8 in col. 2 line 40-42 et seq.

As per Claim 18. Yamawaki et al. discloses method as claimed in claim 17, further comprising the steps of: arraying said data and said error correcting codes in a matrix of plural rows and plural columns; and calculating external code error correcting codes for all column-directional alignments of data in a column direction, and further internal code error correcting codes for all row-directional alignments of data in a column direction or the external code error correcting codes in col. 2 line 40-42 et seq.

As per Claim 19. Yamawaki et al. discloses method as claimed in claim 17, wherein said error correcting codes are Reed-Solomon codes over GF (2.sup.n) in col. 5 lines 43/56.

As per Claim 20. Yamawaki et al. discloses method as claimed in claim 17, wherein said data are arrayed in a matrix of plural rows and plural columns, and a total data length corresponds to a number of symbols, which is equal to or multiply of 2064 in col. 2 line 40-42 et seq.

As per Claim 21. Yamawaki et al. discloses method as claimed in claim 17, wherein said data are arrayed in a matrix of plural rows and plural columns, and a total data length corresponds to a number of symbols which is equal to or multiply of 33024 in col. 2 line 40-42 et seq.

As per Claim 22. Yamawaki et al. discloses method as claimed in claim 17, wherein said data are arrayed in a matrix of plural rows and plural columns, and a total data length of the rows corresponds to a number of symbols which is equal to or multiply of 192 in col. 2 line 40-42 et seq.

As per Claim 23. Yamawaki et al. discloses method as claimed in claim 17, wherein said data are arrayed in a matrix of plural rows and plural columns, and a total data length of the columns corresponds to a number of symbols which is equal to or multiply of 172 in col. 2 line 40-42 et seq.

As per Claim 24. Yamawaki et al. discloses method as claimed in claim 18, wherein external code error correcting codes are isolated into a first block comprising even number rows and a

second block comprising odd number rows in col. 2 line 40-42 et seq.

As per Claim 25. Yamawaki et al. discloses method as claimed in claim 24, wherein calculations of said external code error correcting codes are made with a row-directional increment of 2 or more integer in col. 2 line 40-42 et seq.

As per Claim 26. Yamawaki et al. discloses method as claimed in claim 17, wherein calculations of said error correcting codes are made with a second column-directional increment of 2 or more integer in col. 2 line 40-42 et seq.

As per Claim 27. Yamawaki et al. discloses method as claimed in claim 17, further comprising the steps of: arraying said data and said error correcting codes in a matrix array of plural rows and plural columns; dividing said data and said error correcting codes into a plurality of sectors; and adding at least an additional information to each of said sectors to form each logic segment in col. 2 line 40-42 et seq.

As per Claim 28. Yamawaki et al. discloses method as claimed in claim 27, wherein said each segment has a segment size of 2048 bytes in col. 2 line 40-42 et seq.

As per Claim 29. Yamawaki et al. discloses method as claimed in claim 27, wherein said each segment has a segment size of 2064 bytes, which comprises 2048 bytes for data and 16 bytes for segment header in col. 2 line 40-42 et seq.

As per Claim 30. Yamawaki et al. discloses method as claimed in claim 27, wherein each external code error correcting code is placed following to an end of said each sector in col. 2 line 40-42 et seq. and col. 5 line 65.

As per Claim 31. Yamawaki et al. discloses method as claimed in claim 27, wherein each external code error correcting code is placed on a center region of said matrix array in col. 2 line 40-42 et seq.

As per Claim 32. Yamawaki et al. discloses method as claimed in claim 15, wherein a length of

said each symbol is equal to a bit length of coded data in col. 2 line 40-42 et seq.

As per Claim 33. Yamawaki et al. discloses table or memory means including at least data and error correcting codes, wherein a total code length including said data and said error correcting codes corresponds to not less than 256 symbols, and each of said symbols comprises n-bits, where n is larger than 8 in col. 2 line 40-42 et seq.

As per Claim 34. Yamawaki et al. discloses table or memory means as claimed in claim 33, wherein said table comprises a matrix array of said data and said error correcting codes over plural rows and plural columns; and said error correcting codes includes external code error correcting codes for all column-directional alignments of data in a column direction, and internal code error correcting codes for either one of all row-directional alignments of data in a column direction or the external code error correcting codes in col. 2 line 40-42 et seq. and col. 5 line 65.

As per Claim 35. Yamawaki et al. discloses table or memory means as claimed in claim 33, wherein said error correcting codes are Reed-Solomon codes over GF (2.sup.n) in and col. 5 line 65.

As per Claim 36. Yamawaki et al. discloses table or memory means as claimed in claim 33, wherein said table has a data array of plural rows and plural columns, and a total data length corresponds to a number of symbols, which is equal to or multiply of 2064 in col. 2 line 40-42 et seq.

As per Claim 37. Yamawaki et al. discloses table or memory means as claimed in claim 33, wherein said table has a data array of plural rows and plural columns, and a total data length corresponds to a number of symbols which is equal to or multiply of 33024 in col. 2 line 40-42 et seq.

As per Claim 38. Yamawaki et al. discloses table or memory means as claimed in claim 33, wherein said table has a data array of plural rows and plural columns, and a total data length of

the rows corresponds to a number of symbols which is equal to or multiply of 192 in col. 2 line 40-42 et seq.

As per Claim 39. Yamawaki et al. discloses table or memory means as claimed in claim 33, wherein said table has a data array of plural rows and plural columns, and a total data length of the columns corresponds to a number of symbols which is equal to or multiply of 172 in col. 2 line 40-42 et seq.

As per Claim 40. Yamawaki et al. discloses table or memory means as claimed in claim 34, wherein external code error correcting codes are isolated into a first block comprising even number rows and a second block comprising odd number rows in col. 5 line 65.

As per Claim 41. Yamawaki et al. discloses table or memory means as claimed in claim 33, wherein said table has a matrix array comprising said data and said error correcting codes over plural rows and plural columns, and said matrix array has a plurality of logic segments, and each of said logic segments includes each sector and an additional information, and said each sector including at least one of said data and said error correcting codes in col. 5 line 65.

As per Claim 42. Yamawaki et al. discloses table or memory means as claimed in claim 41, wherein said each segment has a segment size of 2048 bytes in col. 2 line 40-42 et seq.

As per Claim 43. Yamawaki et al. discloses table or memory means as claimed in claim 41, wherein said each segment has a segment size of 2064 bytes, which comprises 2048 bytes for data and 16 bytes for segment header in col. 2 line 40-42 et seq.

As per Claim 44. Yamawaki et al. discloses table or memory means as claimed in claim 41, wherein each external code error correcting code is positioned following to an end of said each sector in col. 2 line 40-42 et seq.

As per Claim 45. Yamawaki et al. discloses table or memory means as claimed in claim 41, wherein each external code error correcting code is positioned on a center region of said matrix

array in col. 2 line 40-42 et seq.

As per Claim 46. Yamawaki et al. discloses table or memory means as claimed in claim 45, wherein a length of said each symbol is equal to a bit length of coded data in col. 2 line 40-42 et seq.

As per Claim 47. Yamawaki et al. discloses table or memory means as claimed in claim 33, wherein said table comprises an error correcting code block table in col. 2 line 40-42 et seq. and col. 5 line 65.

As per Claim 48. Yamawaki et al. discloses table or memory means as claimed in claim 33, wherein said table has a size larger than 256. times.256 arrays of symbols in col. 2 line 40-42 et seq.

As per Claim 49. A system for recording and transmitting digital data, wherein said system includes a table as claimed in claim 33 in col. 2 line 40-42 et seq.

As per Claim 50. Yamawaki et al. discloses method of using a table as claimed in claim 33 in col. 2 line 40-42 et seq.

Claim Rejections - 35 USC § 112 SECOND PARAGRAPH

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3.1 It is not clear to the Examiner what step is used in claims 1, 17, 33, 50 and intervening claims.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

4.1 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-0755. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre

Guy J. Lamarre, P.E
Primary Examiner
July 23,7/24/04